Engineering Cryptographic Software

An introduction to the Cortex-M4

Radboud University, Nijmegen, The Netherlands

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Our platform: Arm

- Company designs CPUs, does not build them
- Market leader for mobile devices, embedded systems

- ARMv7E-M architecture
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- STM32F407VGT6
  - Cortex-M4 + peripherals
- 1024 KB flash
- 192 KB SRAM
- 168 MHz CPU

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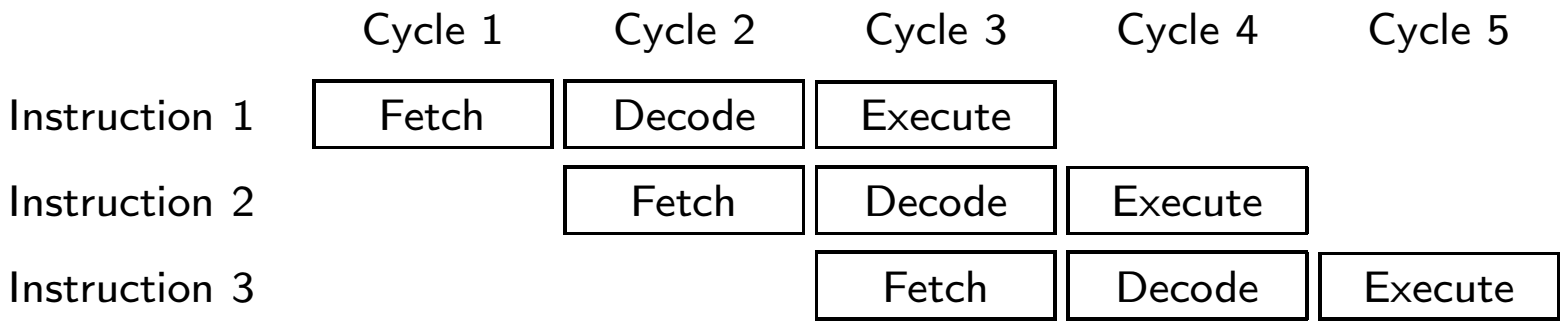

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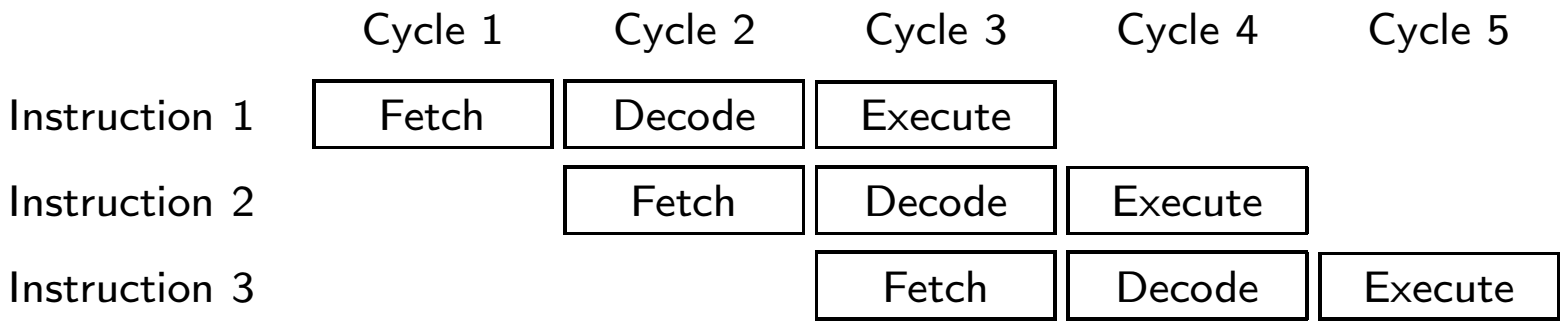

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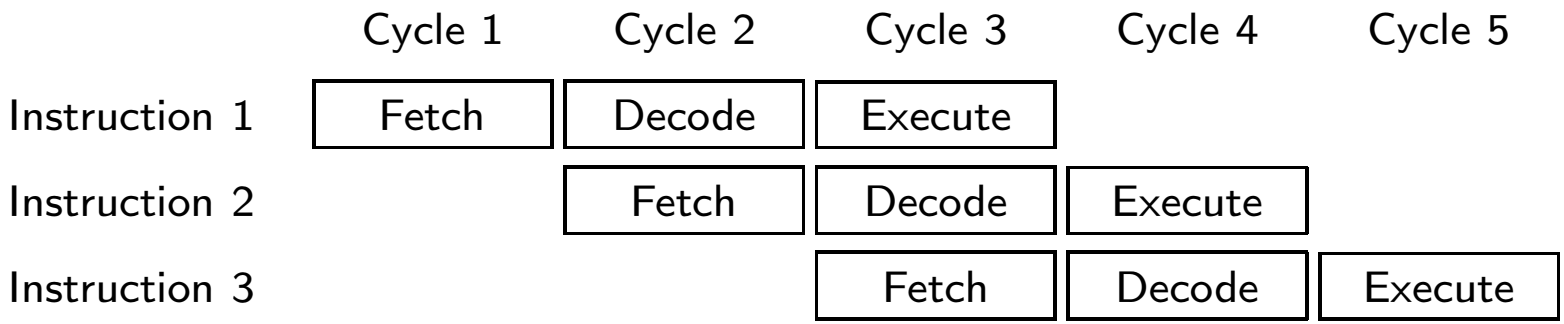

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- Execute happens in one cycle: dependencies do not cause stalls

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- Lookups from constant tables go through cache $\rightarrow$ **timing leakage!**
- Binaries also run on Cortex-M7, which has cached access to RAM

- Write "constant-time" code!
  - No branching on secret data
  - No memory access at secret locations

Registers

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- `r0`–`r12` are general purpose and can be freely used

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- Shifts/rotates: `ror`, `lsl`, `lsr`, `asr`
- All have variants with registers as operands and with a constant ('immediate')

Combined barrel shifter

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- Two instructions for the price of one, only costs 1 cycle
- Optimized code uses this all the time
- Possible with most arithmetic instructions

Barrel shifter example

Possible:

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mov r0, #42
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ror r1, r1, #1
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More efficient:

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- Barrel shifter does not update `Rm`, i.e. `r1` and `r2`!

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  - `bge` *label* (`r0 >= r1`, signed)
  - And many more

Conditional branches (example)

- In C:

```
uint32_t a, b = 100;

for (a = 0; a <= 50; a++) {
    b += a;
}
```

- In asm:

```
mov r0, #0      // a
mov r1, #100    // b

loop:
add r1, r0    // b += a

add r0, #1    // a++
cmp r0, #50   // compare a and 50
bls loop      // loop if <=
```

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- Can load from the stack without moving `sp` (in a few slides)
- Not popping all pushed values will crash the program

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somedata:
    .word 0x01234567, 0xfedcba98
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- For global constants in ROM/flash, use `.section .rodata`

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- `ldm/stm r0!, {r1,r2,r5}` [...] and increments r0
- `push {r0,r1}` == `stmdb sp!, {r0,r1}`
  - *'store multiple decrement before'*

Subroutines

```
somelabel:
    add r0, r1
    add r0, r1, ror #2
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    bx lr

main:
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- Some performance overhead due to branching

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- For *private* subroutines: can ignore this ABI

Architecture Reference Manual

- Large PDF that includes all of this, and more
- Available online: https://developer.arm.com/documentation/ddi0403/eb/
- See Chapter A7 for instruction listings and descriptions

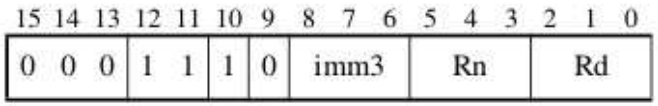
Architecture Reference Manual

A6.7.3 ADD (immediate)

This instruction adds an immediate value to a register value, and writes the result to the destination register. It can optionally update the condition flags based on the result.

Encoding T1 All versions of the Thumb ISA.

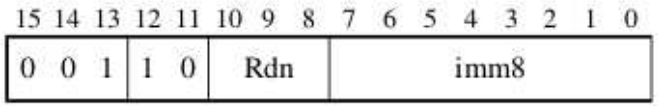
```
ADDS <Rd>,<Rn>,#<imm3>          Outside IT block.
ADD<c> <Rd>,<Rn>,#<imm3>        Inside IT block.
```




```
d = UInt(Rd);  n = UInt(Rn);  setflags = !InITBlock();  imm32 = ZeroExtend(imm3, 32);
```

Encoding T2 All versions of the Thumb ISA.

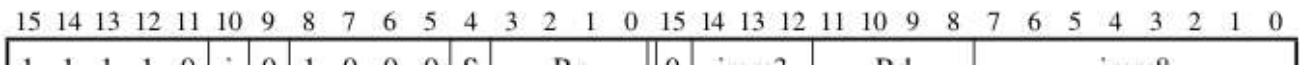
```
ADDS <Rdn>,#<imm8>              Outside IT block.
ADD<c> <Rdn>,#<imm8>            Inside IT block.
```




```
d = UInt(Rdn);  n = UInt(Rdn);  setflags = !InITBlock();  imm32 = ZeroExtend(imm8, 32);
```

Encoding T3 ARMv7-M

```
ADD{S}<c>.W <Rd>,<Rn>,#<const>
```



Architecture Reference Manual

Assembler syntax

```
ADD{S}<c><q>  {<Rd>,} <Rn>, #<const>
ADDW<c><q>  {<Rd>,} <Rn>, #<const>
```

where:

S	If present, specifies that the instruction updates the flags. Otl update the flags.
<c><q>	See *Standard assembler syntax fields* on page A6-7.
<Rd>	Specifies the destination register. If <Rd> is omitted, this reg
<Rn>	Specifies the register that contains the first operand. If the Sl *(SP plus immediate)* on page A6-26. If the PC is specified fc
<const>	Specifies the immediate value to be added to the value obta allowed values is 0-7 for encoding T1, 0-255 for encoding T See *Modified immediate constants in Thumb instructions* o allowed values for encoding T3.

Time to get to work!

- If you haven't "walked through" the STM32F4 getting started, do so.
- If you never wrote assembly before, download this example in your assignment folder:
  `https://github.com/denigreco/crypto_engineering_asm_example.git`
- Otherwise, start working on ChaCha20
- These slides are also on the course website